Claims

[c1] 1. A network, comprising:
a first processor including a first processor data channel;
a first hybrid switching module (HSM) including a first HSM processor data channel coupled with the first processor data channel, a first HSM first bridge, a first HSM redundant bus controller (RBC) coupled with the first HSM first bridge, wherein the first HSM RBC includes a first HSM peer RBC channel, and a first HSM first main bus channel coupled with the first HSM first bridge;
a first main bus coupled with the first HSM first main bus channel, such that the first HSM first bridge bridges communication between the first processor and the first HSM first main bus when authorized by the first HSM RBC;
a second RBC having a second RBC peer RBC channel coupled with the first HSM RBC peer RBC channel; and
a second processor including a second processor data channel coupled with the first main bus such that data is communicated between the second processor and the first main bus when the first HSM RBC is in standby.

[c2] 2. The network as claimed in claim 1, further comprising:
a second HSM including the second RBC, a second HSM processor data channel coupled with the second processor data channel, and a second HSM bridge coupled with the second RBC, wherein the second HSM bridge includes a second HSM main bus channel coupled with the first main bus such that the second HSM bridge bridges communication between the second processor and the first main bus when authorized by the second RBC.

[c3] 3. The network as claimed in claim 2, wherein the first HSM RBC communicates first HSM RBC state information to the second RBC.

[c4] 4. The network as claimed in claim 3, wherein the second RBC communicate second RBC state information to the first HSM RBC.

[c5] 5. The network as claimed in claim 1, wherein the first HSM including a first HSM input/output (I/O) link channel;
a third processor having a third processor data channel; and
a third HSM including a third HSM processor data channel coupled with the third

processor data channel, a third HSM I/O link channel coupled with the first HSM I/O link channel, and a third HSM switch that selectively couples with the third HSM processor data channel and selectively couples with the third HSM I/O link channel, wherein the third HSM processor data channel is thereby selectively coupled with the third HSM I/O link channel.

[c6] 6. The network as claimed in claim 5, wherein the first HSM including a first HSM switch that selectively couples with the first HSM first bridge and couples with the first HSM I/O link channel, wherein the first HSM I/O link channel is thereby selectively coupled with the first HSM first bridge.

[c7] 7. The network as claimed in claim 5, wherein the first HSM including a first HSM switch such that the first HSM switch selectively couples with the first HSM processor data channel, the first HSM first bridge and the first HSM I/O link channel, wherein the first HSM processor data channel is thereby selectively coupled to the first HSM first bridge and selectively coupled to the first HSM I/O link channel.

[c8] 8. The network as claimed in claim 1, further comprising:
a third HSM including a third HSM RBC, a third HSM main bus channel, a third HSM bridge which couples with the third RBC and with the third HSM main bus channel, a third HSM I/O link channel, and a third HSM switch selectively coupled with the third HSM bridge and selectively coupled with the third HSM I/O link channel;
a third main bus coupled with the third HSM main bus channel; and
the first HSM including a first HSM I/O link channel coupled with the third HSM I/O link channel, and a first HSM switch selectively coupled with the first processor data channel and selectively coupled with the first HSM I/O link channel, wherein the first HSM processor data channel is thereby selectively coupled with the third HSM main bus channel.

[c9] 9. The network as claimed in claim 1, wherein the first HSM including a first HSM second bus data channel and a first HSM second bridge coupled with the first HSM second bus data channel.

[c10] 10. The network as claimed in claim 9, wherein the first HSM including a first HSM switch coupled with the first HSM processor data channel, selectively coupled with the first HSM first bridge and selectively coupled with the first HSM second bridge coupled, wherein the first HSM processor data channel is thereby selectively coupled with the first HSM first bridge and selectively coupled with the first HSM second bridge.

[c11] 11. A system, comprising:
a first processor;
a first hybrid switching module (HSM) coupled with the first processor and a first main bus, wherein the first processor accesses the first main bus through the first HSM;
the first HSM includes a first HSM redundant bus controller (RBC);
a second processor coupled with the first main bus; and
a second RBC coupled with the first HSM RBC, wherein the second RBC grants the second processors control over the first main bus when the first HSM RBC is inactive.

[c12] 12. The network as claimed in claim 11, further comprising:
a second HSM that includes the second RBC, wherein the second processor couples with the second HSM and accesses the first main bus through the second HSM.

[c13] 13. The network as claimed in claim 11, further comprising:
a third HSM including a third HSM input/output link (I/O link);
a third processor coupled with the third HSM; and
the first HSM including a first HSM I/O link coupled with the third HSM I/O link, wherein the third processor accesses the first main bus through the third HSM and the first HSM.

[c14] 14. The network as claimed in claim 13, further comprising:
a second main bus coupled with the third HSM, such that the third processor accesses the second main bus through the third HSM.

[c15] 15. The network as claimed in claim 11, further comprising:

a fourth processor coupled with the first main bus;
the fourth processor including a fourth processor RBC coupled with the first HSM RBC and the second RBC, wherein the fourth processor RBC controls access of the fourth processor to the first main bus when the first HSM RBC and second RBC are inactive.

[c16] 16. An apparatus for providing information flow over a data bus, comprising:
a redundant bus controller (RBC);
a first bridge having a first main bus channel, wherein the first bridge couples with the RBC; and
a switch selectively coupled with the first bridge, wherein the first bridge bridges data between the first main bus channel and the switch when directed by the RCB.

[c17] 17. The apparatus as claimed in claim 16, wherein the switch includes a host channel, such that the switch selectively couples the host channel with the first bridge.

[c18] 18. The apparatus as claimed in claim 16, wherein the switch includes a host channel and an input/output (I/O) link channel, such that the switch selectively couples the host channel with the I/O link channel.

[c19] 19. The apparatus as claimed in claim 18, wherein the switch is configured to couple with a remote switch through the I/O link channel.

[c20] 20. The apparatus as claimed in claim 16, wherein the RBC couples with a remote RBC such that the first bridge bridges data between the first main bus channel and the switch when the remote RBC is in standby.

[c21] 21. The apparatus as claimed in claim 16, wherein the RBC includes a peer RBC channel, wherein the peer RBC channel couples with a remote RBC such that the RBC and the remote RBC communicate over the peer RBC channel.

[c22] 22. The apparatus as claimed in claim 16, further comprising:
a second bridge having a second bus channel, wherein the switch selectively couples with the second bridge, such that the second bridge bridges

communication between the second bus channel and the switch.

[c23] 23. An apparatus for controlling access to a bus, comprising:
a peer coupling to communicate state information;
a control and status register; and
a sequencer to transition the state of the apparatus.

[c24] 24. The apparatus as claimed in claim 23, further comprising:
a register interface coupled with an arbiter.

[c25] 25. The apparatus as claimed in claim 24, wherein the register interface includes an arbiter state.